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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/841,189	04/25/2001	Govind Malalur	108339-00000	3654

32294 7590 07/08/2005

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EXAMINER	
NGUYEN, BRIAN D	
ART UNIT	**PAPER NUMBER**
2661	

DATE MAILED: 07/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/841,189	MALALUR ET AL.	
	Examiner	Art Unit	
	Brian D. Nguyen	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/18/04 & 4/25/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-9, 14-22, and 27-32 are rejected under 35 U.S.C. 102(a) as being anticipated by LEVEL ONE (Level One™ IXP1200 Network Processor).

Regarding claim 1, Level One discloses a network switch (see figure 1) comprising a first and a second data port interfaces (see a total of 16 ports including 10Mb/100Mb/1Gb, ATM, T1/E1 ports in figure 1 and second paragraph on page 7) a CPU interface (see PCI Bus Unit connected to Host CPU in figure 1), a common memory(see SDRAM and SRAM Memory units in figure 1 and 8K Data Cache in figure 2), a memory management unit (see memory management unit in the right column of page 1), and at least two set of communication channels for communicating data and messaging information wherein one set of communication channels provides communication from the first and second interfaces to the memory management unit and another set provides communication from the memory management unit to the first and second interfaces (see figure 1 where bi-directional communication between elements of the switch is shown, the communication includes data and messaging information, see also channels coupled to the write and read buffers in figure 2); and wherein the first data port interface, the second data port interface, the CPU interface, the common memory, the memory management

unit and the at least two sets of communication channels are embodied in a single substrate (all of these elements are embodied in a single chip (substrate) (see figure 1 and page 1).

Regarding claims 2 and 3, Level One discloses three communication channels including a first channel for communicating data, a second channel for controlling the transmission of data on the first channel, and a third channel for controlling other activity in the switch (see pages 45-50 where different channels are shown).

Regarding claim 4, Level One discloses a gigabit data port interface (see figure 1).

Regarding claim 5, Level One discloses ASIC chip (see first paragraph on page 1).

Regarding claims 6 and 7, Level One discloses the switch is configured to perform layer two/three switching at wire speed (see processor description on page 5).

Regarding claims 8 and 9, Level One discloses a remote CPU (see CPU in figure 1).

Regarding claims 14-22, claim 14-22 are means plus function claims that have substantially the same limitations as the respective apparatus claims 1-9. Therefore, they are subject to the same rejection.

Regarding claims 27-32, claims 27-32 are method claims that have substantially the same limitations as the respective method claims 1-9. Therefore, they are subject to the same rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10-11, 13, 23-24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over LEVEL ONE (Level One™ IXP1200 Network Processor) in view of Hegde (6,570,875).

Regarding claims 10-11 and 13, Level One discloses different tables (see pages 1 and 2.4 on page 11). Level One does not specifically disclose VLAN table. However, a switch that supports VLAN with VLAN table is well known in the art. Hegde discloses VLAN table (see figure 3 and col. 6, lines 1-3). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the VLAN table as taught by Hegde in the system of Level One so that data packets can be routed between VLANs.

Regarding claims 23-24 and 26, claims 23-24 and 26 are means plus function claims that have substantially the same limitations as the respective apparatus claims 10-11 and 13. Therefore, they are subject to the same rejection.

5. Claims 12 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over LEVEL ONE (Level One™ IXP1200 Network Processor) in view of Bray et al (6,483,849).

Regarding claim 12, Level One does not specifically disclose an auto-negotiating unit. However, this feature is well known in the art. Bray discloses an auto-negotiating unit (see figure 2). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the auto-negotiating unit as taught by Bray in the system of Level One so that different devices with different speed can communicate with the switch.

Regarding claim 25, claim 25 is a means plus function claim that has substantially the same limitations as the respective apparatus claim 12. Therefore, it is subject to the same rejection.

Response to Arguments

6. Applicant's arguments filed 5/2/05 have been fully considered but they are not persuasive.

The applicant argued that *the present invention provides a network device that utilizes two sets of communications channels, such that one channel ferries data from ports of the switch to memory and the other channel ferries data from the memory to the ports and that the prior art of LEVEL ONE, Hegde and Bray do not disclose all of the elements of any of the presently pending claims.* The examiner disagrees because LEVEL ONE clearly teaches two sets of communications channels (see bi-directional communication between the data ports and the elements within the switch in figure 1 and figure 2 where two sets of channels are separately shown as write and read; see also full duplex communication in paragraph 2 of page 7). The applicant also argued that *claims 1, 14 and 27 recite, in part, that "the first data port interface, the second data port interface, the CPU interface, the common memory, the memory management unit and the at least two sets of communication channels are embodied on a single substrate. Looking to Figure 1 of LEVEL ONE and its associated description, the "10/100/1Gb Ethernet MAC" and the "ATM, T1/E1, Other MAC" are discussed, but those interfaces are not on the IXP 1200 Network Processor. Both are clearly disclosed as being extemal to the IXP 1200 Network Processor. The network processor does have an "IX Bus Interface Unit" and a "PCI Bus Unit" but if those units were taken as equivalent to the first and second data port interfaces, there would be no disclosure of the CPU interface by LE VEL ONE.* The examiner disagrees, the PCI Bus Unit is for interfacing to the Host CPU and the PCI MAC Devices, and the IX Bus

Interface Unit is for interfacing to 10/100/1Gb Ethernet devices, ATM devices, and other devices (see second paragraph on page 7 where LEVEL ONE support sixteen 10/100 ports at full line rate, full duplex. Note that a single wire connecting an external device to the switch can also be considered an interface). The applicant also argued that *In addition, no memory is disclosed as being resident in the IXP 1200 Network Processor; rather the SDRAM, SRAM, Boot ROM and the peripherals are disclosed as being external to the IXP 1200 Network Processor. Also, internal to the IXP 1200 Network Processor, a single bus connects the IX Bus Interface Unit with the PCI Bus Unit. While the rejection points to the IX Bus, discussed at pages 45-50, as having different channels, the bus would not connect the elements resident on the network device.* The examiner disagrees, because SDRAM, SRAM and Boot ROM are external but SDRAM Memory Unit, SRAM Memory Unit and data cache as shown in figure 2 are internal memories. Note that a single bus comprises a plurality of conductors and two different conductors can carry different signals in different direction, for example, one from the memory to the ports and the other from the ports to the memory.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian D. Nguyen whose telephone number is (571) 272-3084. The examiner can normally be reached on 7:30-6:00 Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (571) 272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

6/28/05

BRIAN NGUYEN
PRIMARY EXAMINER